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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/865,873	05/25/2001	Cheng-Liang Ding	263/225	5100

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EXAMINER	
SHARON, AYAL I	

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 03/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/865,873	DING ET AL.	
	Examiner	Art Unit	
	Ayal I Sharon	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 January 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *5/25/2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Introduction

1. Claims 1-7 of U.S. Application 09/865,873, originally filed on 05/25/2001 are presented for examination. The amendment filed on 1/7/2005 amends the specification, as well as Claims 1,4, and 7.

Drawings

2. This application has been filed with informal drawings which are acceptable for examination purposes only. Formal drawings will be required when the application is allowed. Figures 1-4 contain hand-written text.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. The prior art used for these rejections is as follows:

5. Wang et al., U.S. Patent 6,446,249. (Henceforth referred to as "**Wang**").

6. The claim rejections are hereby summarized for Applicant's convenience. The detailed rejections follow.

7. **Claims 1-7 are rejected under 35 U.S.C. 102(e) as being anticipated by Wang.**

8. In regards to Claim 1, Wang teaches the following limitations:

1. A method of compiling a netlist description of a logic design for programming into a hardware logic emulation system, the netlist description comprising combinational logic gates, sequential logic gates, data paths and clock paths, the sequential logic gates comprising flip-flops and latches, each of the flip-flops comprising a data input, a clock inputs and an output, the method comprising:

compiling the netlist description to create an emulation netlist, said compiling step comprising:
(Wang, especially: col.2, lines 1-9 and col.3, lines 13-30)

identifying every flip-flop in the emulation netlist;
(Wang, especially: col.3, lines 13-30 "The improved circuit has a logic element having a RAM, lookup table, optional delay element and flip flop /latch.")

changing the emulation netlist such that an adjustable delay element is disposed at the data input of each of the flip-flops of the netlist description; and
(Wang, especially: See Fig.11, Item 114; and Abstract, lines 4-8; and col.9, lines 24-25 "... an optional delay element 116 and a programmable flip-flop/latch 140)

after said compiling step, setting a delay for said adjustable delay element to a value that eliminates the possibility of a hold time violation.
(Wang, especially: col.11, lines 45-50 – "A hold time violation may be alleviated by adding the delay at the data path source, by extending the clock CK 114 to output Q 120 time of the previous stat's flip/flop latch 140 ...

and col.13, lines 47-54 - "... it delays the data output slightly to help compensate for clock skew ... thus ensuring hold time.")

col.13, lines 12-20 "... By adjusting the amount of delay introduced by delay element 116, the system can relieve the hold time requirement on the flip-flop/latch 140, allowing the input signal to change earlier without causing a hold time violation.")

9. In regards to Claim 2, Wang teaches the following limitations:

2. The method of claim 1 wherein said adjustable delay comprises a first flip-flop and a second flip flop,

(Wang, especially: col.13, lines 12-20 "One example embodiment of the delay element 116 is a pair of edge-triggered flip-flops connected in series and clocked by the FAST clock 112 ... By adjusting the amount of delay introduced by delay element 116, the system can relieve the hold time requirement on the flip-flop/latch 140, allowing the input signal to change earlier without causing a hold time violation.")

wherein said first flip-flop has an input, an output and a clock input,
(Wang, especially: col.13, lines 12-20 "...a pair of edge-triggered flip-flops connected in series and clocked by the FAST clock 112 ...")

said second flip-flop has an input, an output and a clock input,
(Wang, especially: col.13, lines 12-20 "...a pair of edge-triggered flip-flops connected in series and clocked by the FAST clock 112 ...")

said output of said first flip-flop in communication with said input of said second flip-flop.
(Wang, especially: col.13, lines 12-20 "...a pair of edge-triggered flip-flops connected in series and clocked by the FAST clock 112 ...")

10. In regards to Claim 3, Wang teaches the following limitations:

3. The method of claim 2 wherein said delay is established in said adjustable delay element by varying frequencies input to said clock input on said first flip-flop and to said clock input on said second flip-flop.
(Wang, especially: col.13, lines 12-20 "... By adjusting the amount of delay introduced by delay element 116, the system can relieve the hold time requirement on the flip-flop/latch 140, allowing the input signal to change earlier without causing a hold time violation.")

11. In regards to Claim 4, Wang teaches the following limitations:

4. A method processing a netlist description of a logic design for programming into an emulation system that eliminates hold time violations, the netlist description comprising combinational logic gates, sequential logic gates, data paths and clock paths, the sequential logic gates comprising flip-flops and latches, each of the flip-flops comprising a data input, a clock inputs and an output, the emulation system comprised of programmable logic chips interconnected together, the method comprising:

compiling the netlist description to create an emulation netlist, said compiling step comprising inserting an adjustable delay element at the data input of each of the flip-flops of the netlist description;
(Wang, especially: col.2, lines 1-9 and col.3, lines 13-30)

calculating data path delay time and clock path delay time, the clock paths and data paths may be passing through multiple of the programmable logic chips;
(Wang, especially: col.13, lines 35-40. "The FAST clock 112 is used to clock the delay element 116 so that the delay introduced by the delay element 116 can be

precisely controlled. The FAST clock 112 is also used to clock the timing correction logic 298 (seeFigs. 15, 21) in the flip/flop latch.")

calculating clock skew value between a pair of flip-flops; and
(Wang, especially: col.13, lines 47-54. "... it delays the data output slightly to help compensate for clock skew to any subsequent flip flop stages in the emulated circuit, thus ensuring hold time.")

setting a delay value for said adjustable delay element that makes said data path delay greater than said clock skew.
(Wang, especially: col.13, lines 47-54. "... it delays the data output slightly to help compensate for clock skew to any subsequent flip flop stages in the emulated circuit, thus ensuring hold time.")

12. In regards to Claim 5, Wang teaches the following limitations:

5. The method of claim 4 wherein said adjustable delay comprises a first flip-flop and a second flip flop,
(Wang, especially: col.13, lines 12-20 "One example embodiment of the delay element 116 is a pair of edge-triggered flip-flops connected in series and clocked by the FAST clock 112 ... By adjusting the amount of delay introduced by delay element 116, the system can relieve the hold time requirement on the flip-flop/latch 140, allowing the input signal to change earlier without causing a hold time violation.")

wherein said first flip-flop has an input, an output and a clock input,
(Wang, especially: col.13, lines 12-20 "...a pair of edge-triggered flip-flops connected in series and clocked by the FAST clock 112 ...")

said second flip-flop has an input, an output and a clock input,
(Wang, especially: col.13, lines 12-20 "...a pair of edge-triggered flip-flops connected in series and clocked by the FAST clock 112 ...")

said output of said first flip-flop in communication with said input of said second flip-flop.
(Wang, especially: col.13, lines 12-20 "...a pair of edge-triggered flip-flops connected in series and clocked by the FAST clock 112 ...")

13. In regards to Claim 6, Wang teaches the following limitations:

6. The method of claim 5 wherein said delay is established in said adjustable delay element by varying frequencies input to said clock input on said first flip-flop and to said clock input on said second flip-flop.
(Wang, especially: col.13, lines 12-20 "... By adjusting the amount of delay introduced by delay element 116, the system can relieve the hold time requirement on the flip-flop/latch 140, allowing the input signal to change earlier without causing a hold time violation.")

14. In regards to Claim 7, Wang teaches the following limitations:

> 7. The method of claim 4 further comprising removing selected ones of said adjustable delay elements from the netlist description where said data path delay already greater than said clock skew without setting said delay value.
> (Wang, especially: col.13, lines 47-54. "... it delays the data output slightly to help compensate for clock skew to any subsequent flip flop stages in the emulated circuit, thus ensuring hold time.")

Response to Amendment

Re: Specification

15. In the amendment filed 1/7/2005, applicants have amended paragraph 56 of the specification to remove the phrase "Dennis: review this." Examiner finds that this amendment does not add new matter, and is therefore entered into the record.

Re: Claim Rejections - 35 USC § 102

16. Applicants unpersuasively argue in the amendment filed 1/7/2005 (see p.6) that:

> Wang does not teach a method for compiling a user's design so that the design can be emulated in an emulator to eliminate timing problems.

Applicants then note in a footnote (see p.6) that:

> Wang only discusses the fact that rapid compilation of a user's design is desirable.

Examiner respectfully disagrees. Wang teaches the following (col.1, lines 47-67, emphasis added):

> In contrast, in a logic emulation, prototyping or computing application, the priorities are different. The logic chip is normally part of a larger, multi-chip system, often with tens or hundreds of logic chips. ***Large input design netlists must be automatically compiled*** into all these logic chips with a very high degree of success and a minimum of user intervention. A netlist is a description of a logic design that specifies the components of the design (e.g., the logic gates) and how the components

> are interconnected. Each "net" of a netlist defines a circuit path between pins on a component or an input/output pad. It is essential that the logic chip used in these applications provide routing resources which are flexible and capable enough to nearly always succeed in allowing most of the logic resources to be used by a fully automatic compile process. ***This compile process should execute rapidly.*** Fast compile times minimize the time required to get from the time the user's design is presented to the emulator system to the time all the logic chips are programmed and ready to run the user's design (i.e., emulate the user's design).

Wang therefore teaches that the netlists must be compiled, and the compile process should execute rapidly. Wang's disclosure shows that compilation a user's design was not only well known in the art at the time the invention was made, but was inherent in the logic emulation process

17. Applicants unpersuasively argue in the amendment filed 1/7/2005 (see p.6) that:

> Wang does not teach or suggest identifying every flip-flop in the emulation netlist, which is required by independent claims 1 and 4.

Examiner respectfully disagrees. Wang teaches the following (col.1, lines 47-67, emphasis added):

> In contrast, in a logic emulation, prototyping or computing application, the priorities are different. The logic chip is normally part of a larger, multi-chip system, often with tens or hundreds of logic chips. Large input design netlists must be automatically compiled into all these logic chips with a very high degree of success and a minimum of user intervention. ***A netlist is a description of a logic design that specifies the components of the design (e.g., the logic gates) and how the components are interconnected. Each "net" of a netlist defines a circuit path between pins on a component or an input/output pad.*** It is essential that the logic chip used in these applications provide routing resources which are flexible and capable enough to nearly always succeed in allowing most of the logic resources to be used by a fully automatic compile process. This compile process should execute rapidly. Fast compile times minimize the time required to get from the time the user's design is presented to the emulator system to the time all the logic chips are programmed and ready to run the user's design (i.e., emulate the user's design).

Therefore, the flip-flops, which are "components of the design", are inherently in the netlist.

18. Applicants unpersuasively argue in the amendment filed 1/7/2005 (see p.7) that

> Likewise, Wang does not teach or suggest changing the netlist of the circuit being tested to insert a variable delay element at the data inputs of the all of the flip-flops located in the emulation netlist ...

Examiner respectfully disagrees. Examiner refers the Applicants to the Abstract and col.3, lines 12-35 of Wang. The Abstract teaches the following (emphasis added):

> A circuit for an emulation system that has a logic element having a RAM, lookup table, ***optional delay element*** and flip-flop/latch. The flip-flop/latch may behave as a flip-flop or as a latch and has separate set and reset signals. ***The delay element inserts a selectable amount of delay into the data path of the logic element in order to reduce race time problems.*** The logic elements may be combined to share input signals so as to increase the size of the RAM. The improved circuit also has a playback memory used to store up to a plurality of copies of sampled data from a logic element so that emulation data can be played back for debugging purposes. Multiple read ports coupled to the logic elements permit a user to read out data from the logic elements during emulation in a time multiplexed manner. The input/output pins may be time multiplexed to carry multiple signals, unidirectionally or bidirectionally.

Examiner finds that the highlighted teachings directly contradict Applicants' arguments.

19. Applicants unpersuasively argue (p.7, emphasis added) that

> Instead, the variable delay element of claims 1 and 4 are **inserted into the emulation netlist**, which as discussed is compiled from the netlist provided by the user. In contrast, the delay element in Wang is part of the logic element that **is a building block for the integrated circuits used to build an emulator** ...

In the footnote to this argument, Applicants argue that:

> Wang makes it clear that the logic element disclosed therein is a building block of a programmable logic chip that [is] used to physically build the emulator. See e.g., Col.1, lines 48-67 and Col.2, line 66 through Col.3, line 6.

Examiner respectfully disagrees. The full text of Wang's teachings at the cited Col.1, lines 48-67, is as follows (emphasis added):

> In contrast, in a logic emulation, prototyping or computing application, the priorities are different. The logic chip is normally part of a larger, multi-chip system, often with tens or hundreds of logic chips. ***Large input design netlists must be automatically compiled into all these logic chips with a very high degree of success and a minimum of user intervention.*** A netlist is a description of a logic design that specifies the components of the design (e.g., the logic gates) and how the components are interconnected. Each "net" of a netlist defines a circuit path between pins on a component or an input/output pad. It is essential that the logic chip used in these applications provide routing resources which are flexible and capable enough to nearly always succeed in allowing most of the logic resources to be used by a fully automatic compile process. This compile process should execute rapidly. Fast compile times minimize the time required to get from the time the user's design is presented to the emulator system to the time all the logic chips are programmed and ready to run the user's design (i.e., emulate the user's design).

Therefore, Examiner finds that the "emulation netlist" in Applicants' argument corresponds to "the integrated circuits used to build a generator" in Applicants' argument.

20. Applicants unpersuasively argue (emphasis added) that "Applicant notes that the rejection of claim 7 actually demonstrates why all of the claims are allowable."

More specifically, Applicants argue (see amendment filed 1/7/2005, p.8):

> As discussed above, the Office Action consistently argues that the delay element that form[s] a portion of the logic elements disclosed in Wang are the same as the claimed adjustable delay elements. However, the delay element in Wang is *fabricated* into the programmable logic device, meaning that it *cannot* be removed, as is required by claim 7. That the delay element in Wang is hardwired into the chip is seen by reference to

> Fig.9 of Wang, which is described as "a block diagram of the logical structure of the embodiment of *the emulation chip*". See Col.4, lines 42-43. This block diagramshows "Les", which are the logic elements illustrated in Fig.11 and described at Columns 9-13. Given that the logic elements in Wang are fabricated into the emulation chip described in Wang, structures within that logic element such as the delay element cannot be removed from that logic element. Thus, Wang cannot possibly teach that the adjustable delay elements can be inserted and removed *since they are always present!* **Applicant respectfully submits that Wang does not anticipate any of the claims in this application because Wang does not teach anything about inserting or removing adjustable delay elements into from an emulation netlist that will be programmed into an emulation system.**

Examiner respectfully disagrees. Wang teaches at Col.1, lines 47-67 (emphasis added):

> In contrast, in a logic emulation, prototyping or computing application, the priorities are different. The logic chip is normally part of a larger, multi-chip system, often with tens or hundreds of logic chips. ***Large input design netlists must be automatically compiled into all these logic chips with a very high degree of success and a minimum of user intervention.*** A netlist is a description of a logic design that specifies the components of the design (e.g., the logic gates) and how the components are interconnected. Each "net" of a netlist defines a circuit path between pins on a component or an input/output pad. It is essential that the logic chip used in these applications provide routing resources which are flexible and capable enough to nearly always succeed in allowing most of the logic resources to be used by a fully automatic compile process. This compile process should execute rapidly. Fast compile times minimize the time required to get from the time the user's design is presented to the emulator system to the time all the logic chips are programmed and ready to run the user's design (i.e., emulate the user's design).

It is old and well known in the art that design elements can be added and/or removed from the design netlists before the compilation stage. More specifically, Wang also specifically teaches the optional insertion of the delay element as "... a logic element for a logic block of an integrated circuit for use in an emulation system" (see col.3, lines 12-35, emphasis added):

> Various separate aspects of the invention can be found in an improved circuit for an emulation system. The improved circuit has a logic element having a RAM, lookup table, **optional delay element** and flip flop/latch. The flip/flop latch may behave as a flip flop or as a latch and has separate set and reset signals. The delay element inserts a selectable amount of delay into the data path of the logic element in order to reduce race time problems. The logic elements may be combined to share input signals so as to increase the size of the RAM. The improved circuit also has a shadow memory used to store sampled data from a logic element and to playback emulation data for debugging purposes. Multiple read ports permit a user to read out data from the improved circuit during emulation in a time multiplexed manner. The input/output pins may be time multiplexed to carry multiple signals, unidirectionally or bidirectionally. The improved circuit also has a hold time algorithm to reduce race time problems.
>
> **A first, separate aspect of the invention is a logic element for a logic block of an integrated circuit for use in an emulation system where the logic element includes a delay element that inserts an adjustable amount of delay into the data path of the logic element**.

Examiner finds that these teachings directly contradict Applicants' arguments.

21. Finally, Examiner noted in the previous Office Action that the circuit in Wang's Fig.11 is identical to the circuit in Applicants' Fig.3. Therefore, the behaviors of the circuit in Wang's Fig.11 are inherently identical to the circuit in Applicants' Fig.3.

Conclusion

22. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ayal I. Sharon whose telephone numbers are (703) 306-0297 *[Before Oct. 25, 2004]* and (571) 272-3714 *[After Oct. 25, 2004].* The examiner can normally be reached on Monday through Thursday, and the first Friday of a biweek, 8:30 am – 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached at (703) 305-9704 *[Before Oct. 25, 2004]* and (571) 272-3716 *[After Oct. 25, 2004].*

Any response to this office action should be faxed to (703) 872-9306 or mailed to:

Director of Patents and Trademarks
Washington, DC 20231

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Tech Center 2100 Receptionist, whose telephone number is (703) 305-3900 *[Before Oct. 25, 2004]* or (571) 272-2100 *[After Oct. 25, 2004]*.

Ayal I. Sharon

Art Unit 2123

March 14, 2005